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Functional Verification of AMBA AHB LITE Interconnect using Systemverilog

Pallavi T lambe[1], Meghana Kulkarni[2]

PG Student [VLSI] Dept. ECE, Center of PG studies VTU belagavi, India[1]

Associate Professor Dept. ECE, Center of PG studies VTU belagavi, India[2]

ABSTRACT: Verification is the important part of SoC manufacturing, it gives particular implementation and functionality to DUT for check whether it has achieved specification or not. In this paper communication interconnect i.e. AHB LITE interconnect is verified by developing the reusable verification intellectual property (VIP) using hardware verification language Systemverilog. The AHB LITE is the on-chip-interconnect which manages the functional block in SoC design and develops lossless communication between master and each slave in the SoC design. It also finds the presence of error/bug in the design by generating simulation result and the coverage report using the QUESTA SIM tool.

KEYWORDS: SoC, Systemverilog, AHB LITE, functional verification, QUESTA SIM tool.

I. INTRODUCTION

Due to day by day increase in the complexity of SoC design, verification has become the vital bottleneck in the design technique because it explores correct/incorrect functioning of AHB LITE interconnect in the SoC design. AMBA 3 AHB LITE is the subset of AMBA 2 AHB used in such a SoC design where only one master, one slave or multiple slaves are required like cortex M. There are many approaches of verification of DUT some of these are. In the first approach, the verification of AHB LITE interconnect with wait transfer is carried out and verification environment is developed using UVM methodology. The simulation result of read/write transfer (burst transfer, burst type, burst size) at wait state is explored but coverage report is not covered in verification [1]. In the second approach, the verification of AXI2OCP Bridge is done, which connects two interconnect in SoC design where AXI based processor and the controller based OCP are used [2]. In another approach, the verification of AHB master which is formal based verification but, it is not possible to verify the chip formally because it is math based verification [3].
In this paper Verification IP model is developed and inserted into test bench to simulate and justify the functional correctness of the SoC interconnect (or full SoC design). The simulation result and 100% coverage report of generated test cases using Systemverilog are given.

II.AMBA AHB LITE INTERCONNECT

The AHB LITE is the third version of advanced microcontroller bus architecture (AMBA) introduced by ARM Ltd. Original AHB specification was part of AMBA 2 AHB, some features are removed and named as AHB LITE. The specifications of AMBA 3 AHB LITE are

- Support High performance, high clock frequency and high bandwidth operation.
- Supports only one master and one or more than one slave.
- Separates bus for read and write transfer.
- Support pipelined operation, burst transfer.
- Support only one master so, no need of arbitration.
- No need of master-to-slave multiplexer.
- Support single clock edge operation and non-tristate implementation.

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III.AMBA AHB LITE DESIGN

Designing with the AHB LITE interconnect requires the following components:

1. Master
2. Slave
3. Address decoder
4. Multiplexer

The block diagram for AHB LITE interconnects is shown in Figure 1, with four components i.e.: single master, three slaves, address decoder and slave to master multiplexer. The bus interconnect logic between master to slave consists of one address decoder and multiplexer.

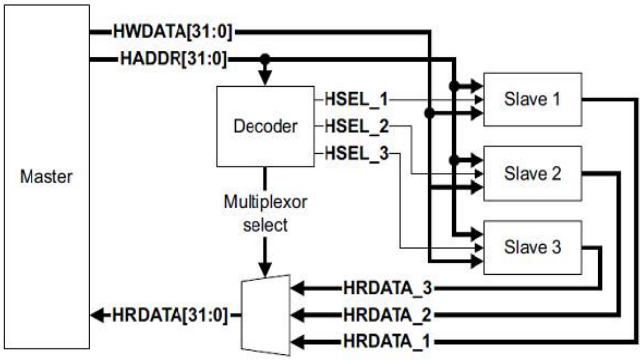

Figure 1: Block diagram of AMBA AHB LITE interconnect

The AHB LITE interconnect supports data bus configuration from 8-bit to 1024-bits but microcontroller supports up to 32-bits data configuration. The 32-bits Address and Control signal sent out of AHB LITE master goes to AHB LITEslave as well as address decoder. Decoder calcifies the transaction to particular AHB LITE slave depending upon the address sent from the AHB-LITE master. Same information is sent to the multiplexer and it will know that which response and data signal mux to the AHB LITE master. At single transfer only one slave will accept the information and other two remains in de-active state. Explanation of each component of Figure 1 is given below:

3.1 AHB LITE Master

The AHBLITE master is the device connected to high throughput bus which gives control and address information to initiate write and read operation. Transfer size of AHB LITE interconnect is fixed which is 32-bits. Figure 2 shows AHB LITE master block diagram which represents the signals of master.

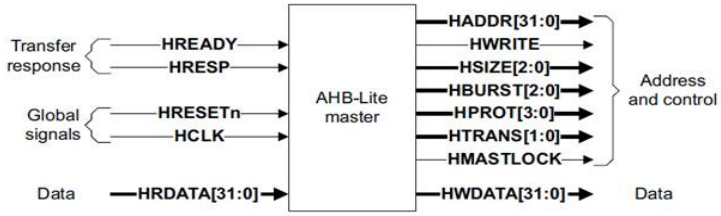

Figure 2: AHB LITE Master

The 32-bit address and data are generated by AHB LITE master to write data into AHB LITE slave and needs control signals for proper data transfer. The signal HADDR, HWRITE, HBURST, HTRANS etc., is generated by AHB LITEmaster and the signals HREADY, HRDATA are received from AHB LITE slave as shown in Figure 2. AHB LITE master starts the operation at positive edge of clock (HCLK). When AHB LITE master selected signal is high, it generates the 32-bit address in the next clock edge and also generates control signal HWRITE, HTRANS to find master to perform read or write operation.

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3.2 AHB LITE Slave

The AHB LITE slave is memory component in the SoC design which captures the data, address from the AHB LITE master and reads the data from its memory location. The AHB LITE slave cannot initiate the operation on its own, it only responds to AHB LITE master. The AHB LITE slave receives the signal from AHB LITE master address decoder and sends the transfer response signal and HRDATA to master.

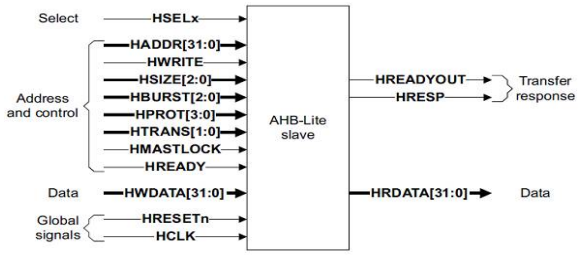

Figure 3: AHB LITE Slave

The AHB LITE slave diagram is shown in Figure 3 which has 32-bit address and control signals from the AHB LITE master and selects signal from the Address decoder and then generates transfer response HREADY, HRESP to AHB LITE master.

3.3 Address decoder

This is the component used when more than two slaves are present in design and it decodes the address of every transfer and gives particular slave signal to AHB LITE slave that is concerned within a transfer. The addresses received from the AHB LITE master are sent to address decoder and particular AHB LITE slave is selected depending on the address coming from AHB LITE master.

3.4 Multiplexer

The multiplexer is used to multiplex the read data and give response signal to AHB LITE master from the AHB LITE slave and also used when number of slave are more than two.

IV. AHB LITE INTERCONNECT VERIFICATION

To know about verification environment of AHB LITE interconnect, the testbench architecture must be known in the broader view. The testbench architecture consists of number of elements which are integrated in the proper way to form a verification intellectual property (VIP). The entire verification process is divided into three parts,

1. Test
2. Verification environment
3. Functional verification

The Figure 3 is the architecture block diagram for AHB LITEinterconnects consists of test case, environment and functional verification.

1) Test – Basically the testcase means, a file which describe the action, event, input and golden (expected) response to find features are correctly working or not. During the development of verification environment it is important to start modelling design input, output and create a memory to store these test. And then these test cases are sent to the generator in testbench architecture.

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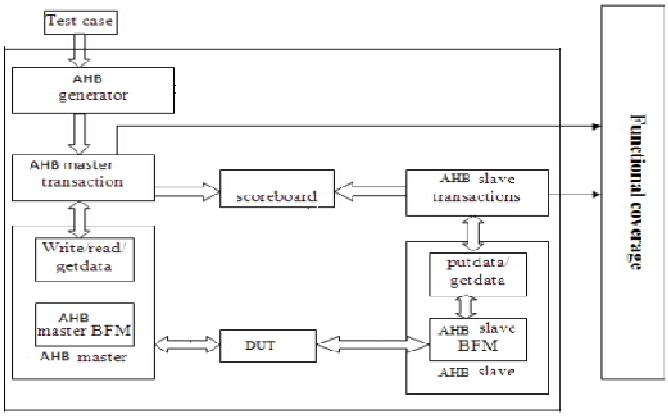

Figure 3: Architectural block diagram for AHB lite interconnect

2) Verification Environment - The verification environment is required to verify the functional correctness of the DUT by driving and creating the input sequence and capturing output of design to compare with golden (expected) output. In the verification environment, separate components are used to perform the specific task and the components are shown in Figure 3.

Generator - Generator generate random testcases and the Systemverilog provide construct to manage random generator order and distribution. These testcases are transferred to the master agent.

Master agent – It is also called as connector/transaction which connects the AHB LITE driver, generator, scoreboard and the functional coverage. It also controls configuration operation of DUT and convert high level information achieved from generator (burst transfer) into the individual command.

Master driver – It gets the data from master agent and drives on DUT by converting into actual input of DUT. It achieves back response from design under test and again converts response in object format to send master agent.

The slave agent and slave driver working is same as master agent and master driver.

Scoreboard – It is also known as tracker, consists of reference model in which the expected output is stored. As the random stimuli from generator is sent to DUT and the same stimuli are sent to the scoreboard and saved into DUT till it gives the output. Then the scoreboard compares the actual output and the golden output and gives the result of verification.

3) Functional coverage – It is the one which introduces how much functionality of design is covered. Some features of functional verification are

- Explains which feature in verification checked successfully.
- In verification which part of feature checked and how much it is close to complete verification.
- Gives confidence that the previously fixed design will not re-produce bugs.

V. SIMULATION RESULT

Using hardware verification language i.e. Systemverilog simulationbeing carried out. The simulation waveform and coverage report are analysed by running the generated testcases for the multiple operation. The main application of Systemverilog is re-useability of code for multiple test scenarios. And the testcases are used to verify the AHB LITE interconnect.The HREADY signal is active, master drives 32-bit address, 32-bit data and slave accept it after half clock cycle with starting address and the data are zero, starting burst type is single, starting burst transfer is idle and burst transfer size is 3'h0 shown in figure 3. The write transfer and read transfer will not continue at same clock cycle. When master sends data to slave 0 the remaining two slaves remain in de-active state as shown in Figure 4.

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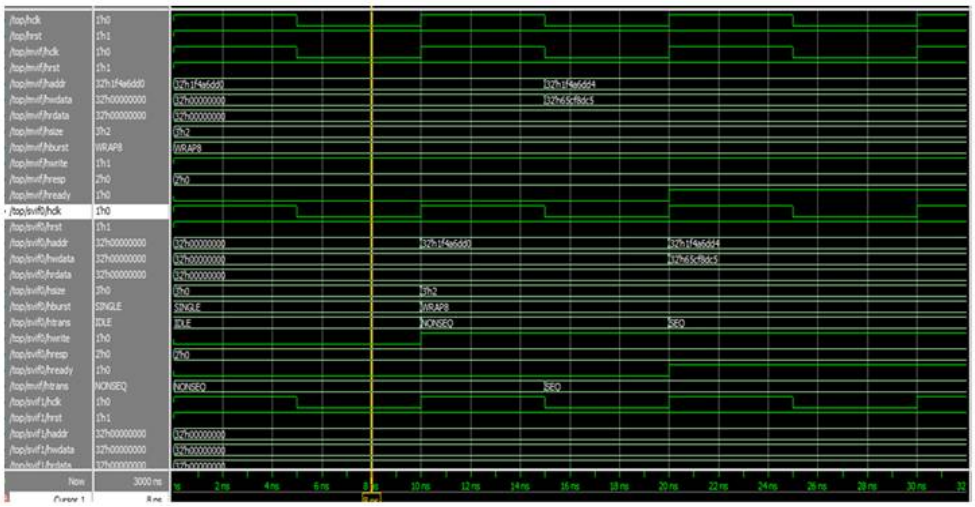

Figure 4: Simulation result when S0 is in active state

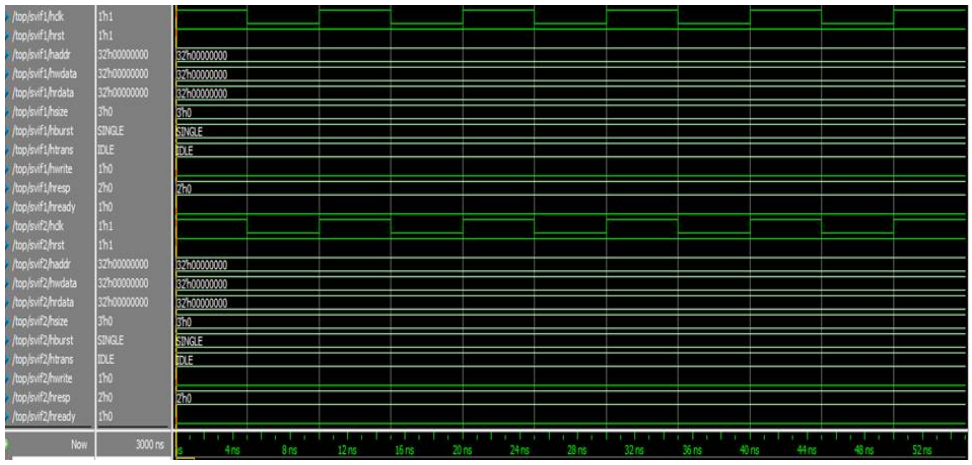

Figure 4: Simulation result when S1, S2 are in de-active state

Write operation – The write operation with burst transfer, HREADY signal is high and the HWRITE is also high.The write address and data values are passed to module with burst wraping, incrementing (4,8 and 16) are shown in figure 5.When master sends 32-bit address[32'h1f4a6dd0,32'h1fa6dd4……..] and 32-bit write data[32'h00000000,32'h65cfadc5……], slave (S0) receives this address and data after half clock period, shown in below Figure 5.

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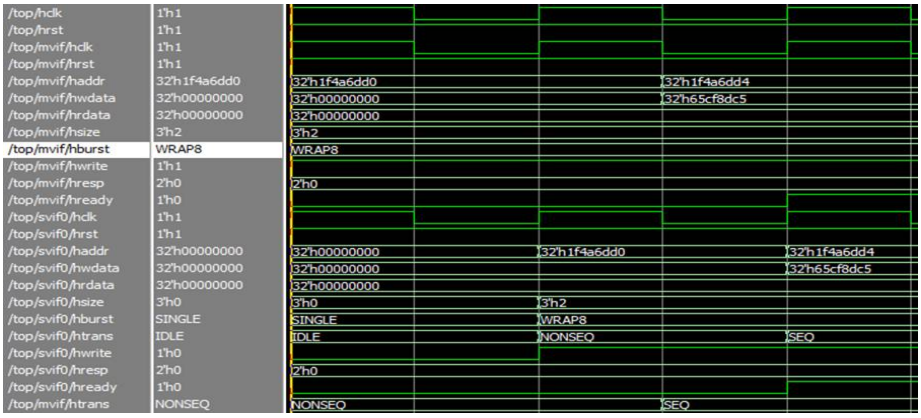

Figure 5: Burst write operation

Read operation – After completion of write operation, the read operation will continue with a burst transfer. At read transfer the HREADY is high and HWRITE is low as shown in below Figure 6.

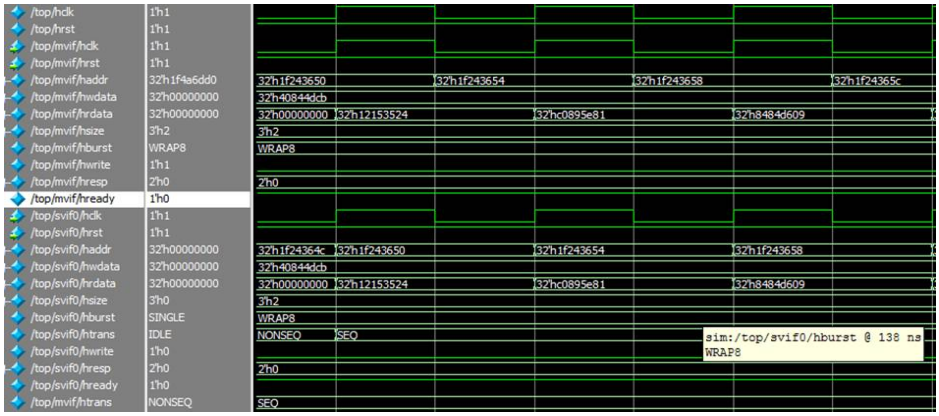

Figure 6: Burst read operation

Coverage report – The 100% coverage report for AHB LITE interconnects is shown in below Figure 7 which covers all the test cases which are generated in verification architecture.

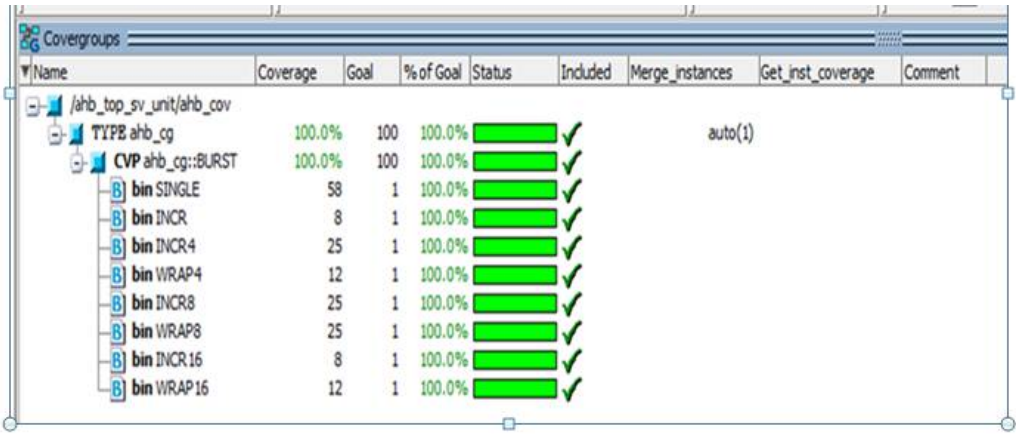

Figure 7: Coverage report

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VI.CONCLUSION

In this paper, code for AHB LITE interconnect environment is simulated and output is observed. The functional verification of the AHB LITE interconnects, simulation waveforms developed by the Mentor Graphics QUESTA SIM tool and explored as per expectation without any change in the features of DUT.The environment totally wraps DUT under verification and observes the optimum functional, and coverage is functional based coverage.Bins have been created based on the constraints and 100% functional coverage has been obtained on them. The 100% functional coverage report is given by developing the re-usable VIP and by generating the testcases for AHB LITE interconnect. The result is achieved on the latest version of tool i.e., QUESTA SIM 64 10.C tool.

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